CLAIMS

1. A method of conditional branching in a pipelined processor, the method comprising the steps of:

(A) prefetching a branch target address in response to encountering a branch instruction, in prediction of taking a branch; and

(B) evaluating between (i) taking said branch and (ii) not taking said branch substantially contemporaneously with prefetching said branch target address.

2. The method of claim 1, further comprising the steps of:

prefetching a sequential instruction address in response to evaluating to take said branch; or

prefetching a mispredict recovery address in response to evaluating not taking said branch.

3. The method of claim 2, further comprising the step of:

generating said sequential instruction address based upon a program counter address and a predetermined offset.

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4. The method of claim 2, further comprising the step of:

generating said misprediction recovery address based upon an exception program counter address and a second predetermined offset.

5. The method of claim 1, further comprising the step of:

generating said branch target address based upon a program counter address and an address displacement of said branch condition.

6. The method of claim 1 further comprising the steps of:

generating a sequential instruction address based upon a program counter address and a predetermined offset;

generating a misprediction recovery address based upon an exception program counter address and a second predetermined offset;

generating said branch target address based upon a program counter address and an address displacement of said branch condition;

prefetching said sequential instruction address in response to evaluating to take said branch; and

prefetching said mispredict recovery address in response to evaluating not taking said branch.

7. A pipelined processor comprising:

a multiplexer; and

a circuit configured to present (i) a branch target address to said multiplexer in prediction of taking a branch and (ii) a mispredict recovery address to said multiplexer when not taking said branch.

8. The pipelined processor of claim 7, wherein said circuit is further configured to present a sequential instruction address to said multiplexer when taking said branch.

9. The pipelined processor of claim 7, further comprising:

a prefetch program counter for storing a program counter address presented by said multiplexer and used in generating said sequential instruction address.

10. The pipelined processor of claim 7, further comprising:

a prefetch program counter for storing a program counter address presented by said multiplexer and used in generating said branch target address; and

an instruction register for storing said branch instruction used in generating said branch target address.

11. The pipelined processor of claim 7, further comprising:

an exception program counter disposed in a decode stage of said pipelined processor for storing an exception program counter address used in generating said mispredict recovery address.

12. The pipelined processor of claim 7, further comprising:

an exception program counter disposed in an execution stage of said pipelined processor for storing an exception program counter address used in generating said mispredict recovery address.

13. The pipelined processor of claim 7, further comprising:

said circuit being further configured to provide a sequential instruction address to said multiplexer for use upon choosing to take said branch;

a prefetch program counter for storing a program counter address presented by said multiplexer and used in generating said sequential instruction address and said branch target address;

an instruction register for storing said branch instruction used in generating said branch target address; and

an exception program counter for storing an exception program counter address used in generating said mispredict recovery address.

14. A pipelined processor comprising;

a means for multiplexing;

a means for presenting a branch target address to said means for multiplexing in prediction of taking a branch; and

a means for presenting a mispredict recovery address to said means for multiplexing when not taking said branch.